Paper No. 21

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte DAVID ROBERT BALDWIN

Appeal No. 2005-0217
Application No. 09/591,226

HEARD: June 8, 2005

Before HAIRSTON, GROSS, and BARRY, *Administrative Patent Judges*.
BARRY, *Administrative Patent Judge*.

A patent examiner rejected claims 1-6. The appellant appeals the rejection of claims 1, 3, 4, and 6 under 35 U.S.C. § 134(a).[1] We affirm-in-part.

I. BACKGROUND

The invention at issue on appeal handles texture data used by rendering accelerators for three-dimensional ("3D") graphics. 3D graphics are aimed at displaying a realistic view of a 3D scene on the monitor of a computer. Elements of a 3D scene are defined by sets of polygons (typically triangles), each having attributes

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[1]At oral hearing, the appellant's attorney withdrew the appeal of claims 2 and 5.

such as color, reflectivity, and spatial location. For example, a person is translated into a few hundred triangles which map out the surface of his body. (Spec. at 1.)

A 3D graphics pipeline comprises a stage for geometry and a stage for rendering. The geometry stage manages polygon activities and converts 3D spatial data into a two-dimensional ("2D") representation of a viewed scene. (*Id.*) The rendering stage "renders" the 2D representation to produce correct values for all pixels of each frame of an image sequence. "Textures" are used to enhance the visual appeal of rendering. A texture is a 2D image that is mapped into the data to be rendered. More specifically, textures are employed to generate the level of minor surface detail that makes synthetic images realistic, without transferring immense amounts of data. (*Id.* at 2.)

Virtual memory architectures have long been used in general-purpose computers, (*id.* at 10), to give a user the impression of a memory space that is larger than can be physically accommodated in real memory. Such an impression is achieved by partitioning the memory space into a small physical working set and a large virtual set with dynamic swapping between the two. (*Id.* at 9.) For its part, the appellant's invention manages texture storage in a host memory in addition to the texture storage in normal texture memory. (*Id.* at 10.)

A further understanding of the invention can be achieved by reading the following claims.

1. A graphics processing method, comprising the steps of:

(a.) performing 3D-graphics rendering in a graphics accelerator subsystem, using a dedicated graphics memory as primary memory for rendering accelerator logic;

(b.) using a system main memory as additional memory to hold textures required by said rendering accelerator logic; and

(c.) when textures required by said rendering accelerator logic are not present in said dedicated graphics memory, then either

downloading said textures from main memory into said graphics memory, or

selectively, when commanded by a software application, allowing said accelerator logic to read textures directly from said main memory without downloading them into said graphics memory.

4. The method of Claim 1, wherein said accelerator logic is able to read noncontiguous textures directly from said main memory.

3. A graphics processing chip, comprising:

a graphics accelerator comprising rendering acceleration logic; and

a texture memory management function, integrated on said chip, which manages both texture storage in host memory and also texture storage in normal texture memory.[2]

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[2]"The drawing in a nonprovisional application must show every feature of the invention specified in the claims." 37 C.F.R. § 1.83(a). "Any structural detail that is of

Claims 1 and 4 stand rejected under 35 U.S.C. § 103(a) as obvious over U.S. Patent No. 6,295,068 ("Peddada") and U.S. Patent No. 6,249,853 ("Porterfield"). Claims 3 and 6 stand rejected under § 103(a) as obvious over Porterfield and U.S. Patent No. 6,292,201 ("Chen").

II. OPINION

Our opinion addresses the rejections in the following order:

- claim 1
- claim 4
- claims 3 and 6 .

A. CLAIM 1

Rather than reiterate the positions of the examiner or the appellant *in toto*, we focus on the point of contention therebetween. The examiner asserts, "[i]t would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of Porterfield into Peddada in order to use both AGP models and thus to add the flexibility to the system." (Examiner's Answer at 4.) The

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sufficient importance to be described should be shown in the drawing." M.P.E.P. § 608.02(d) (citing *Ex parte Good*, 1911 C.D. 43, 164 O.G. 739 (Comm'r Pat. 1911)). Here, we were unable to read many of the claimed limitations on the appellant's drawings. We leave the question of satisfaction of the aforementioned authorities to the examiner and the appellant.

appellant argues, "*Peddada et al.* expressly teaches away from the combination. . . ." (Appeal Br. at 13.)

"The presence or absence of a motivation to combine references in an obviousness determination is a pure question of fact." *In re Gartside*, 203 F3d 1305, 1316, 53 USPQ2d 1769, 1776 (Fed. Cir. 2000) (citing *In re Dembiczak*, 175 F.3d 994, 1000, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999)). A suggestion to combine teachings from the prior art "may be found in explicit or implicit teachings within the references themselves, from the ordinary knowledge of those skilled in the art, or from the nature of the problem to be solved." *WMS Gaming Inc. v. Int'l Game Tech.*, 184 F.3d 1339, 1335, 51 USPQ2d 1385, 1397 (Fed. Cir. 1999) (citing *In re Rouffet*, 149 F.3d 1350, 1355, 47 USPQ2d 1453, 1456 (Fed. Cir. 1998)).

Of course, "[w]hen prior art contains apparently conflicting references, the Board must weigh each reference for its power to suggest solutions to an artisan of ordinary skill. The Board must consider all disclosures of the prior art. . . ." *In re Young*, 927 F.2d 588, 591, 18 USPQ2d 1089, 1091 (Fed. Cir. 1991) (citing *In re Lamberti*, 545 F.2d 747, 750, 192 USPQ 278, 280 (CCPA 1976)). In weighing each reference, we "must consider the passages and references which point away from the invention as well as

those said to point toward it." *General Tire & Rubber Co. v. Firestone Tire Co.*, 349 F.Supp. 345, 359, 174 USPQ 427, 445 (N.D. Ohio 1972).

Here, the issue is whether there was a motivation to employ both a direct memory access ("DMA") model and an execute model. Porterfield discloses that the execute model enables a graphics accelerator to "use, or 'execute,' graphics data directly from the memory in which it resides. . . ." Col. 6, ll. 66-67. Regarding the execute model, Peddada discloses, "[u]nfortunately, 3D graphics accelerator 20 must have additional hardware to directly access textures from AGP memory 14. This extra hardware adds to the expense and complexity of 3D graphics accelerator 20 and is thus undesirable." Col. 1, ll. 58-62. We find the use of the adverb "unfortunately" implies that the execute model offers advantages. Among these advantages are the fact that "[s]ome textures should not be downloaded into storage on [a] graphics card, because they will only be used once." (Spec. at 11.) "In such cases the cost of downloading them doesn't compensate for the faster local access." (*Id.*) Furthermore, the examiner's finding, *supra*, that employing both the DMA model and the execute model would offer more flexibility than employing only the DMA model is uncontested. "The appellant's [s]ilence implies assent.'" *Ex parte Knapton,* 67 USPQ2d 1059, 1060 (Bd.Pat.App. & Int. 2002) (quoting *Harper & Row Publishers, Inc. v. Nation Enters.,* 471 U.S. 539, 572, 225 USPQ 1073, 1085 (1985)).

"That a given combination would not be made by businessmen for economic reasons does not mean that persons skilled in the art would not make the combination because of some technological incompatibility. Only the latter fact would be relevant." *In re Farrenkopf*, 713 F.2d 714, 718, 219 USPQ 1, 4 (Fed. Cir. 1983) (citing *Orthopedic Equipment Co. v. United States*, 702 F.2d 1005, 1013, 217 USPQ 193, 200 (Fed. Cir.1983)). Accordingly, we are unpersuaded that the additional expense associated with the execute model would discourage one of ordinary skill in the art from seeking the advantages expected therefrom.

Of course, the added complexity of the execute model would point away from its use. Considering all the aforementioned, however, we find that the advantages of the execute model and the added flexibility of employing both the DMA model and the execute model would have outweighed the complexity associated with the latter. Therefore, we affirm the obviousness rejection of claim 1.

B. CLAIM 4

The examiner finds, "the reading by the accelerator logic of Porterfield is still considered a directly because the meaning of 'directly' here is meaning reading or execute from main memory without copy to the local texture memory." (Examiner's Answer at 7.) The appellant argues, "[a]ssistance from the host CPU is still required

before the *Porterfield* graphics accelerator can read the textures from the main memory." (Appeal Br. at 14.)

In addressing the point of contention, the Board conducts a two-step analysis. First, we construe the claim at issue to determine its scope. Second, we determine whether the construed claim would have been obvious.

1. Claim Construction

"Analysis begins with a key legal question — *what* is the invention *claimed*?" *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561, 1567, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987). In answering the question, "the Board must give claims their broadest reasonable construction. . . ." *In re Hyatt*, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1668 (Fed. Cir. 2000). Furthermore, "[a] transitional term such as 'comprising' or . . . 'which comprises,' does not exclude additional unrecited elements, or steps. . . ." *Moleculon Research Corp. v. CBS, Inc.*, 793 F.2d 1261, 1271, 229 USPQ 805, 812 (Fed. Cir. 1986).

Here, claim 4 recites in pertinent part the following limitations: "said accelerator logic is able to read noncontiguous textures directly from said main memory." Giving the dependent claim its broadest, reasonable construction, the limitations require that

accelerator logic read noncontiguous graphics data directly from a main memory. Because claim 1, from which claim 4 depends, uses the transitional term "comprising," however, it does not exclude additional elements or steps.

2. Obviousness Determination

Having determined what subject matter is being claimed, the next inquiry is whether the subject matter would have been obvious. The question of obviousness is "based on underlying factual determinations including . . . what th[e] prior art teaches explicitly and inherently. . . ." *In re Zurko*, 258 F.3d 1379, 1383, 59 USPQ2d 1693, 1696 (Fed. Cir. 2001) (citing *Graham v. John Deere Co.*, 383 U.S. 1, 17-18, 148 USPQ 459, 467 (1966); *In re Dembiczak*, 175 F.3d 994, 998, 50 USPQ 1614, 1616 (Fed. Cir. 1999); *In re Napier*, 55 F.3d 610, 613, 34 USPQ2d 1782, 1784 (Fed. Cir. 1995)).

Here, Porterfield's "graphics accelerator 160 communicates with . . . main memory 156 through an accelerated graphics port (AGP) 166." Col. 6, ll. 26-29. As mentioned regarding claim 1, the graphics accelerator 160 reads "graphics data directly from the memory in which it resides," *id.* at ll. 65-67, viz., the main memory 156. Because "the main memory 156 is dynamically allocated in random pages of a selected size, such as 4K, the 'execute' model requires an address mapping mechanism to map random pages into a single contiguous, physical address space

needed by the graphics accelerator 160." Col. 7, ll. 1-5. Because claim 1 is open-ended, however, it does not preclude help from the address mapping mechanism in reading the noncontiguous graphics data. Therefore, we affirm the obviousness rejection of claim 4.

C. CLAIMS 3 AND 6

The examiner asserts, "without recited any particular functions of memory managing in the claim to distinguish from memory accessing of Porterfield, the teachings of accessing memory by Porterfield can be considered as memory managing because accessing memory is one of memory managing functions." (Examiner's Answer at 8.) The appellant argues, "the specification and the prosecution history of the present application, as well as the ordinary meaning in the art, all use the term 'memory management' to describe a collection of techniques for providing sufficient memory to one or more processes in a computer system. Therefore, it cannot be maintained that memory management is the same thing as accessing memory." (Reply Br. at 5.)

1. Claim Construction

"Claims are not interpreted in a vacuum, but are part of and are read in light of the specification." *Slimfold Mfg. Co. v. Kinkead Indus., Inc.*, 810 F.2d 1113, 1116, 1

USPQ2d 1563, 1566 (Fed. Cir. 1987) (citing *Hybritech Inc. v. Monoclonal Anti-bodies, Inc.*, 802 F.2d 1367, 1385, 231 USPQ 81, 94-95 (Fed. Cir. 1986); *In re Mattison*, 509 F.2d 563, 565, 184 USPQ 484, 486 (CCPA 1975)). Here, claim 3 recites in pertinent part the following limitations: "a texture memory management function, integrated on said chip, which manages both texture storage in host memory and also texture storage in normal texture memory." For its part, the appellant's specification discloses that "'memory management' logic often performs functions related to virtual memory management as well as to cache management." (Spec. at 4.) Reading the limitations in light of the specification, claim 3 requires functions related to virtual memory management and cache management.

2. Obviousness Determination

"In rejecting claims under 35 U.S.C. Section 103, the examiner bears the initial burden of presenting a prima facie case of obviousness." *In re Rijckaert*, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993) (citing *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992)). "'A prima facie case of obviousness is established when the teachings from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art.'" *In re Bell*, 991 F.2d 781, 783, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993) (quoting *In re Rinehart*, 531 F.2d 1048, 1051, 189 USPQ 143, 147 (CCPA 1976)).

Here, the examiner does not allege, let alone show, that the teachings from Porterfield or Chen would have suggested functions related to virtual memory management and cache management. Because it involves neither virtual memory management nor cache management, we are unpersuaded that "accessing memory is one of memory managing functions." (Examiner's Answer at 8.) Therefore, we reverse the obviousness rejection of claim 3 and of claim 6, which depends therefrom.

III. CONCLUSION

In summary, the rejection of claims 1 and 4 under § 103(a) is affirmed. The rejection of claims 3 and 6 under § 103(a), however, is reversed.

"Any arguments or authorities not included in the brief will be refused consideration by the Board of Patent Appeals and Interferences. . . ." 37 C.F.R. § 1.192(a). Accordingly, our affirmance is based only on the arguments made in the briefs. Any arguments or authorities omitted therefrom are neither before us nor at issue but are considered waived. *Cf. In re Watts*, 354 F.3d 1362, 1367, 69 USPQ2d 1453, 1457 (Fed. Cir. 2004) ("[I]t is important that the applicant challenging a decision not be permitted to raise arguments on appeal that were not presented to the Board.") No time for taking any action connected with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

KENNETH W. HAIRSTON
Administrative Patent Judge

ANITA PELLMAN GROSS
Administrative Patent Judge

LANCE LEONARD BARRY
Administrative Patent Judge

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